DESCRIPTION:

The **1HH01** is a horizontal Hall device that can be incorporated as a cell into an integrated circuit designed for 0.35µm CMOS process.

The output voltage of the 1HH01 is proportional to a magnetic field component perpendicular to the chip surface.

The HH01 cell (or a cluster of such cells) can be readily integrated into a Hall sensor circuit, such as the spinning-current circuit.

KEY FEATURES:

- **Sensitive to magnetic field perpendicular to the chip surface**
- **0.35µm bulk CMOS technology**
- **Small cell size**
- **High signal-to-noise ratio**
- **Interchangeable biasing and sense contacts – suitable for the spinning current circuit**

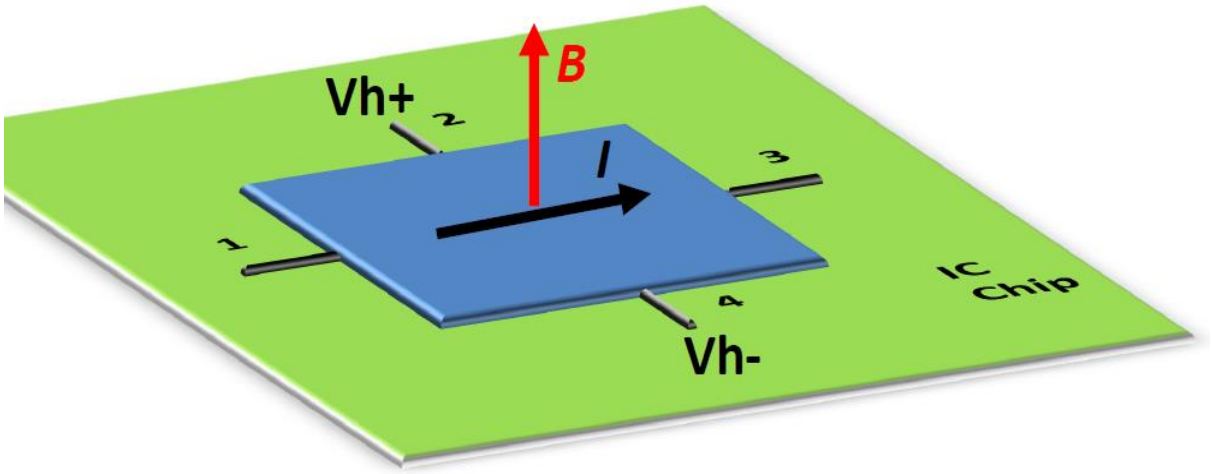

Figure 1. **Illustrating position, biasing, and response of the 1HH01. The active area of the Hall device is an n-type plate-like region, which is imbedded into the p-type substrate of the chip so that the planes of the Hall device and the chip are parallel. Notation: 1, 2, 3, 4 - the current (input) and/or sense (output, Hall voltage) terminals; I – the biasing current; B – the magnetic field induction; Vh+, Vh- – the positive and negative terminals of the Hall voltage generator.**

ABSOLUTE MAXIMUM RATINGS:

Parameter	Value	Remark
Supply voltage range	-0.5V to +6V	*Any terminal (1, 2, 3 or 4) to substrate*
Operating temperature range	-40°C to +125°C	

CHARACTERISTICS:

Unless otherwise noted, the specifications apply for the biasing voltage *V*b (between the current terminals) of 1V, with the „low" biasing terminal connected to the substrate, at the temperature 20°C.

Parameter	Value	Remark
Sensitivity vector	Perpendicular	*With respect to the chip surface*
Dimensions of the cell	15µm x 15µm	*Overall dimensions*
Magnetic sensitive volume	10 x 10 x 1 μm^3	*1µm: Perpendicular to the surface*
Resistance R_{in}, R_{out}	1.6kΩ ±10%	*Between the terminals 1-2 or 3-4*
Offset voltage V_{Off}	±1mV (typical)	*at B = 0T*
Common output voltage V_C	0.48V	*With respect to "low" biasing terminal*
Magnetic sensitivity S_V	0.045V/VT ±3%	*Bias-voltage-related magn. sensitivity*
Magnetic sensitivity S_I	70V/AT ±10%	*Bias-current-related magn. sensitivity*
Noise voltage spectral density	See Figure 2	
Corner frequency of 1/f noise (f_c)	1kHz (typical)	*Where 1/f noise equals thermal noise*
NEMFsd*) at f > 10 x f_c	120nT*V/ $\sqrt{Hz}$ / Vb	*Vb: biasing voltage*

*) *NEMFsd: Noise-equivalent magnetic field spectral density*

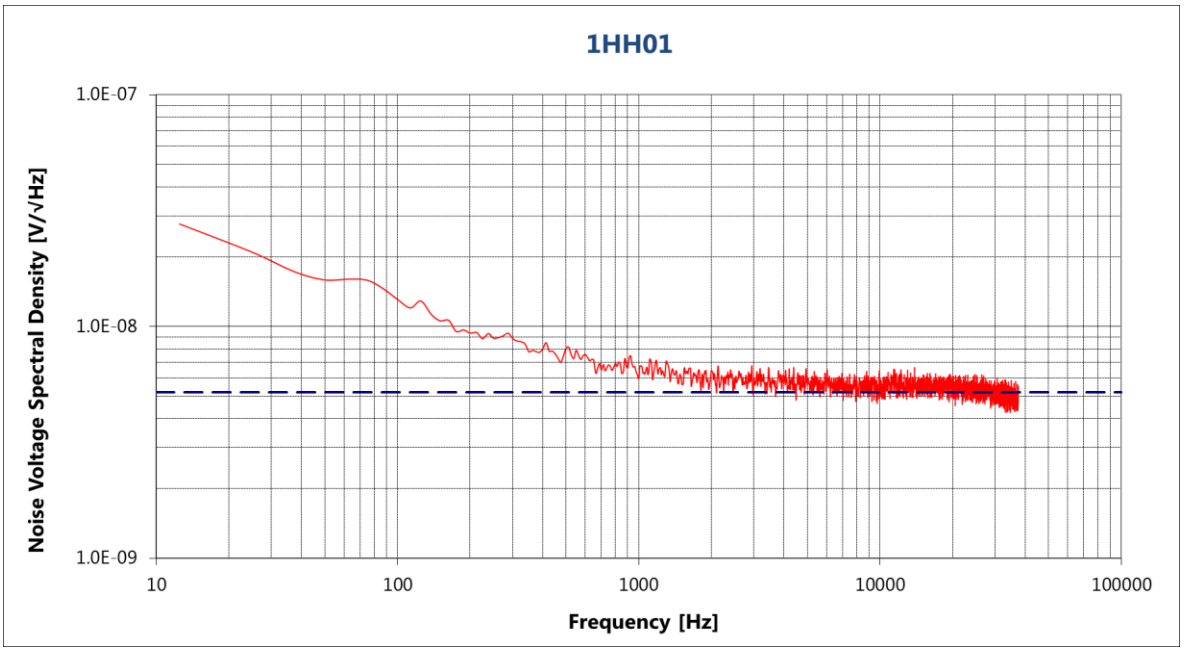

Figure 2. **Noise voltage spectral density of the 1HH01 vs. frequency. The dashed line indicates the thermal noise floor of a 1.6kΩ resistor.**

Note: A cluster of N cells 1HH01 connected in parallel will have the following characteristics:

- Resistance R_{in}, R_{out}: $R_N = R_1/N$;
- Sensitivity $S_{VN} = S_{V1}$, $S_{IN} = S_{I1}/N$;
- Offset $Voff_N = Voff_1 / \sqrt{N}$;
- Noise $Vn_N = Vn_1 / \sqrt{N}$,

where the suffix 1 indicates a value of 1HH01, and N indicates a value of N parallel-connected 1HH01.